AMENDMENTS TO THE CLAIMS:

This listing of the claims will replace all prior versions, and listings, of the claims in this application.

Claim 43 has been canceled without prejudice.

Listing of Claims:

1. (Currently Amended) A computer program product stored on a computer readable storage medium for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, comprising computer readable program code for performing:

in a non-testing mode, the first controller detecting an error in the first controller and thereby initiating a process to maintain data access during failure of the first controller, the process to maintain data access during failure of the first controller comprising:

the first controller instructing the at least one other controller to save the at least one other controller's internal state information;

saving internal state information of the first controller by the first controller;

the first controller resetting itself after the saving of its internal state information;

pausing operation of the at least one other controller; and

the at least one other controller saving its internal state information at the time of pausing, in parallel with the first controller's saving of its internal state information; and

continuing operation of the at least one other controller, wherein only the first controller resets during the process to maintain data access during failure of the first controller, wherein the first and the at least one other controller make the array of data storage devices appear to a host computer as a single high capacity storage device, wherein the internal state information of the

first and the at least one other controller is saved to permit diagnosis of the failure of the first controller, wherein a flag is set when internal status data save operation is occurring to prevent another internal status data save operation from being invoked, wherein the flag is set to prevent the another internal status data save operation from being invoked before the greater time period of a set timeout period and the time period to write the internal status data to a memory.

2. (Previously Presented) A computer program product as claimed in claim 1, wherein the first controller detects an error in the first controller which triggers the saving of the internal state information.

3. (Previously Presented) A computer program product as claimed in claim 1, wherein a host computer issues a transaction to the first controller which causes the first controller to save its internal state information.

4. (Previously Presented) A computer program product as claimed in claim 3, wherein the first controller resets after saving its internal state information.

5. (Canceled).

6. (Previously Presented) A computer program product as claimed in claim 1, wherein the at least one other controller pauses operation, saves internal state information at the time of pausing, and continues operation when the at least one other controller detects a loss of the first controller such that access to the array of data storage devices is maintained.

7. (Previously Presented) A computer program product as claimed in claim 1, wherein the first controller and the at least one other controller each save their internal state information to a storage location corresponding to that controller.

8. (Previously Presented) A computer program product as claimed in claim 1, wherein the first controller and the at least one other controller save their internal state information to at least one storage device.

9. (Previously Presented) A computer program product as claimed in claim 1, wherein the first controller instructs the at least one other controller to transfer internal state information to the

first controller.

10. (Previously Presented) A computer program product as claimed in claim 9, wherein the first controller saves the internal state information of the first controller and of the at least one other controller to the storage devices.

11. (Previously Presented) A computer program product as claimed in claim 1, wherein the first controller and the at least one other controller are combined on a single circuit card.

12. (Previously Presented) A computer program product as claimed in claim 1, wherein in addition to the internal state information, at least one of the first controller and the at least one other controller save external memory data corresponding to an interface chip trace area.

13. (Previously Presented) A computer program product as claimed in claim 1, wherein the at least one other controller saves a subset of internal state information.

14. (Previously Presented) A computer program product as claimed in claim 1, wherein the internal state information saved by the at least one other controller is determined by an instruction received from the first controller.

15. (Previously Presented) A computer program product as claimed in claim 1, wherein problem analysis regarding an error in the first controller is carried out on the saved internal state information.

16. (Previously Presented) A computer program product as claimed in claim 1, wherein the storage subsystem comprises a Fibre Channel Arbitrated Loop system and the first controller and the at least one other controller comprise host bus adapters.

17. (Previously Presented) A computer program product as claimed in claim 16, wherein during the at least one other controller pausing operation, saving internal state information at the time of pausing, and continuing operation, interrupts are disabled.

18. (Previously Presented) A computer program product as claimed in claim 16, wherein a flag is set in a host bus adapter during the saving of internal state information to prevent overlapping saves of internal state information in that adapter.

19. (Previously Presented) A computer program product as claimed in claim 16, wherein the host bus adapter saves information relating to an interface chip trace area.

20. (Currently Amended) A method for maintaining data access during failure of a first controller in a multiple controller storage subsystem, the storage subsystem having an array of data storage devices and at least one other controller for managing the data storage, the method comprising:

in a non-testing mode, the first controller detecting an error in the first controller and thereby initiating a process to maintain data access during failure of the first controller, the process to maintain data access during failure of the first controller comprising:

the first controller saving its internal state information;

pausing operation of the at least one other controller; and

the at least one other controller saving its internal state information at the time of pausing without resetting; and,

continuing operation of the at least one other controller, wherein only the first controller resets during the process to maintain data access during failure of the first controller, wherein the internal state information of the first and the at least one other controller is saved to permit diagnosis of the failure of the first controller, wherein one of the first and at least one other controller records the destination of the saved internal state information of an other of the first and at least one other controller, wherein a flag is set when internal status data save operation is occurring to prevent another internal status data save operation from being invoked, wherein the flag is set to prevent the another internal status data save operation from being invoked before the greater time period of a set timeout period and the time period to write the internal status data to a memory.

21. (Previously Presented) A computer program product as claimed in claim 8, wherein the internal state information is subsequently retrieved from the at least one storage device.

22. (Previously Presented) A computer program product as claimed in claim 1, wherein the first controller and the at least one other controller share a single memory.

23. (Canceled).

24. (Currently Amended) A storage subsystem comprising at least two controllers for managing data storage, the at least two controllers coupled to at least one data storage device, the storage subsystem further comprising:

a first controller of the at least two controllers adapted for saving its internal state information during a failure of the first controller in a non-testing mode, the first controller detecting an error in the first controller and thereby initiating a process to maintain data access during failure of the first controller; and,

at least one other controller of the at least two controllers adapted for pausing its operation, and continuing its operation during the failure of the first controller, wherein only the first controller resets during the process to maintain data access during failure of the first controller, wherein the internal state information of the first and the at least one other controller is saved in order to permit diagnosis of the failure of the first controller, wherein a flag is set when internal status data save operation is occurring to prevent another internal status data save operation from being invoked, wherein the flag is set to prevent the another internal status data save operation from being invoked before the greater time period of a set timeout period and the time period to write the internal status data to a memory.

25. (Canceled).

26. (Canceled).

27. (Previously Presented) A storage subsystem as in claim 24, wherein the first controller and the at least one other controller share an external memory.

28. (Previously Presented) A storage subsystem as in claim 24, wherein at least one of the first controller and the at least one other controller are disposed on a single circuit card.

29. (Canceled).

30. (Previously Presented) A storage subsystem as in claim 24, wherein the storage subsystem comprises a Fibre Channel Arbitrated Loop system and the at least one other controller comprises

a host bus adapter.

31. (Currently Amended) A Fibre Channel Arbitrated Loop storage system comprising:

a first set of disk drives connected to a first set of loops, and a second set of disk drives redundant with the first set of disk drives and connected to a second set of loops; wherein a first adapter is connected to the first set of loops and a second adapter is connected to the second set of loops; each adapter being adapted for issuing a command to the other adapter to save internal status data and not reset itself, wherein each adapter is adapted for saving internal status data and resetting, wherein a flag is set when internal status data save operation is occurring to prevent another internal status data save operation from being invoked, wherein the flag is set to prevent the another internal status data save operation from being invoked before the greater time period of ~~the group consisting of~~ a set timeout period and the time period to write the internal status data to a memory.

32. (Canceled).

33. (Canceled).

34. (Previously Presented) A Fibre Channel Arbitrated Loop storage system according to claim 31, wherein the Fibre Channel Arbitrated Loop storage system has two contexts and two kinds of internal status data save operations.

35. (Previously Presented) A Fibre Channel Arbitrated Loop storage system according to claim 34, wherein the two contexts are a fibre context and an interrupt context and the two kinds of internal status data save operations are a live dump and a dump to disk.

36. (Previously Presented) A Fibre Channel Arbitrated Loop storage system according to claim 35, wherein resets are not permitted during a live dump.

37. (Previously Presented) A Fibre Channel Arbitrated Loop storage system according to claim 35, wherein when one of the first and second adapters live dumps, it sends a message to an other of the first and second adapters to build a data structure recording state information for debugging purposes.

38. (Previously Presented) A computer program product as claimed in claim 1, wherein a subset of the internal state information is saved in order to reduce the period of time the at least one controller is paused and to reduce the amount of storage space used to store the internal state information.

39. (Previously Presented) A Fibre Channel Arbitrated Loop storage system according to claim 16, wherein one of the first and at least one other controller records the destination of a live dump of an other of the first and at least one other controller.

40. (Previously Presented) A Fibre Channel Arbitrated Loop storage system according to claim 39, wherein the controller that records the destination of a live dump provides the destination of the live dump to the other controller when the other controller inquires.

41. (Previously Presented) A storage subsystem as in claim 24, wherein the internal state information of the first controller and the at least two other controllers is stored in a storage buffer of the first controller.

42. (Previously Presented) A storage subsystem as in claim 24, wherein the internal state information of the first controller is stored in a storage buffer of the first controller and the internal state information of each of the at least two other controllers is stored in a storage buffer of a corresponding one of each of the at least two other controllers.

43. (Canceled).